Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-10 (Canceled)

Claim 11 (Previously Presented): An output buffer circuit comprising:

an input terminal for receiving an input signal;

an output terminal for outputting an output signal;

a first inverter connected to the input terminal, the first inverter outputting a first signal having a slow rise up and fall down characteristic;

a second inverter connected to the input terminal, the second inverter outputting a second signal having the slow rise up and fall down characteristic;

a pull up control circuit connected to the input terminal, the pull up control circuit pulling up a voltage of the first signal during a predetermined time from a time when the input signal is changed from "L" level to "H" level;

a pull down control circuit connected to the input terminal, the pull down control circuit pulling down a voltage of the second signal during a predetermined time from a time when the input signal is changed from "H" level to "L" level;

a first output transistor having a source connected to a first power source

potential node, a drain connected to the output terminal and a gate connected to the first inverter so as to receive the first signal; and

a second output transistor having a source connected to a second power source potential node, a drain connected to the output terminal and a gate connected to the second inverter so as to receive the second signal.

Claim 12 (Previously Presented): An output buffer circuit according to claim 11, wherein each of the first and second inverters comprises,

an inverter input terminal;

an inverter output terminal;

a first inverter transistor of a first conductivity type having a back gate connected to the second power source potential node, a first terminal, and a second terminal and a gate connected together with the first power source potential node;

a second inverter transistor of a second conductivity type having a back gate connected to the first power source potential node, a first terminal connected to the first terminal of the first inverter transistor, a second terminal connected to the inverter output terminal and a gate connected to the inverter input terminal;

a third inverter transistor of the second conductivity type having a back gate connected to the first power source potential node, a first terminal, and a second terminal and a gate connected together with the second power source potential node; and

a fourth inverter transistor of the first conductivity type having a back gate connected to the second power source potential node, a first terminal connected to the first terminal of the third inverter transistor, a second terminal connected to the inverter output terminal and a gate connected to the inverter input terminal.

Claim 13 (Previously Presented): An output buffer circuit according to claim 11, wherein each of the first and second inverter comprises,

an inverter input terminal;

an inverter output terminal;

a first inverter transistor of a first conductivity type having a back gate connected to the first power source potential node, a first terminal, a second terminal connected to the inverter output terminal and a gate connected to the inverter input terminal;

a first diode connected between the first power source potential node and the first terminal of the first inverter transistor for pulling down a voltage supplied from the first power source potential node;

a second inverter transistor of a second conductivity type having a back gate connected to the second power source potential node, a first terminal, a second terminal connected to the inverter output terminal and a gate connected to the inverter input terminal; and

a second diode connected between the second power source potential node and the first terminal of the second inverter transistor for pulling down a voltage supplied

from the first terminal of the second inverter transistor.

Claim 14 (Previously Presented): An output buffer circuit according to claim 13, wherein the first diode has an anode connected to the first power source potential node, and a cathode connected to the first terminal of the first inverter transistor, and wherein the second diode has a cathode connected to the second power source potential node, and an anode connected to the first terminal of the second inverter transistor.

Claim 15 (Previously Presented): An output buffer circuit according to claim 11, wherein the pull up control circuit includes,

a delay circuit having an input terminal connected to the input terminal of the output buffer circuit and having an output terminal, and

a pull up transistor having a first terminal connected to the first power source potential node, a second terminal connected to an inverter output terminal of the first inverter and a gate connected to the output terminal of the delay circuit.

Claim 16 (Previously Presented): An output buffer circuit according to claim 11, wherein the pull down control circuit includes,

a delay circuit having an input terminal connected to the input terminal of the output buffer circuit and having an output terminal, and

a pull down transistor having a first terminal connected to the second power

source potential node, a second terminal connected to an inverter output terminal of the second inverter and a gate connected to the output terminal of the delay circuit.

Claim 17 (Previously Presented): An output buffer circuit according to claim 11, further comprising an enable gate circuit having a first input terminal connected to the input terminal of the output buffer circuit, a second input terminal connected to receive an enable signal and a pair of output terminals respectively connected to inverter input terminals of the first and second inverters.

Claim 18 (Previously Presented): An output buffer circuit according to claim 17, wherein the enable gate circuit includes,

an AND circuit having a first input terminal connected to the first input terminal of the enable gate circuit, a second input terminal connected to receive the enable signal and an output terminal connected to the inverter input terminal of the first inverter,

a third inverter having an input terminal connected to receive the enable signal and having an output terminal, and

an OR circuit having a first input terminal connected to the first input terminal of the enable gate circuit, a second input terminal connected to the output terminal of the third inverter and an output terminal connected to the inverter input terminal of the second inverter.

Claims 19-20 (Canceled)